AN2555
Application note

Porting an application from the ST10F269Zx to the ST10F276Z5

Introduction

The ST10F276Z5 is a member of the STMicroelectronics ST10 family of 16-bit single-chip CMOS microcontrollers. It is functionally upward compatible with the ST10F269Zx.

The goal of this document is to highlight the differences between ST10F269Zx and ST10F276Z5 devices. It is intended for hardware or software designers who are adapting an existing application based on the ST10F269Zx to the ST10F276Z5.

This document presents the ST10F276Z5's modified functionalities and the new ones then it describes the modified registers and the new registers. For each part, the differences with the ST10F269Zx that may have an impact when replacing the ST10F269Zx by the ST10F276Z5 are stressed and some advice is given on the way they can be handled.

This document applies from the second silicon version of the ST10F276Z5, that is from the BA step where a new sectorization of the Flash memory was introduced. The silicon version can be verified by reading the IDCHIP register at location 00'F07Ch. The values for these silicon versions are 114Xh with X > 1.

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1 Modified features

1.1 Pinout

1.1.1 Pinout modification summary

Table 1 summarizes the modifications made in the pinout.

Table 1. Pinout modifications

Pin number	ST10F269Zx name and function	ST10F276Z5 name and function
17	DC: Internal voltage regulator decoupling. Connect to nearest V_{SS} via a 330 nF capacitor.	V_{DD}: 5 V power supply pin
56	DC1: Internal voltage regulator decoupling. Connect to nearest V_{SS} via a 330nF capacitor.	V18: Internal voltage regulator decoupling. Connect to nearest V_{SS} via a 10-100nF capacitor.
99	$\overline{EA}$: Selects code execution out of internal Flash memory or external memory according to level during reset.	$\overline{EA}$-V_{STBY}: Selects code execution out of internal Flash memory or external memory according to level during reset. Power supply input for standby mode.
143	V_{SS}: Ground pin	XTAL3: Input to the 32 kHz oscillator amplifier circuit. When not used shall be tied to ground to avoid consumption. Besides, bit OFF32 in RTCCON register must be set.
144	V_{DD}: 5V power supply pin	XTAL4: Output of the 32 kHz oscillator amplifier circuit. When not used must be left open to avoid spurious consumption.

1.1.2 Pin 17

On the ST10F269Zx, a decoupling capacitor of 330nF minimum has to be connected between the pin 17 (named DC2) and the nearest V_{SS} pin.

This is no longer the case for the ST10F276Z5 device where pin 17 is a V_{DD} pin.

Hardware impact

PCB must be adapted.

Software impact

None.

1.1.3 Pin 56

On the ST10F269Zx, a decoupling capacitor of 330nF minimum has to be connected between the pin 56 (named DC1) and the nearest V_{SS} pin.

On the ST10F276Z5, pin 56 is named V_{18} and a capacitor of value between 10nF minimum to 100nF maximum must be connected between it and the nearest V_{SS} pin.

Hardware impact

Change on the capacitor value. As the value is much lower, the footprint of the capacitor might be smaller and a modification of the PCB might be needed.

Software impact

None.

1.1.4 Pin 99

On the ST10F269Zx, pin 99 is $\overline{EA}$ and used upon reset to select the start from the internal Flash memory or the external memory.

On the ST10F276Z5, pin 99 has the additional function of providing the 5V power supply to the device in standby mode (new power-saving mode), it is called $\overline{EA}$-V_{STBY}.

Hardware impact

The modification depends on the previous use of the ST10F269Zx and on whether the Standby mode is used or not.

For an application where the Standby mode is not used, no change to the PCB is required. If the new application uses the Standby mode, the $\overline{EA}$-V_{STBY} pin must be separated from the common 5V and have a specific supply path.

Software impact

None.

1.1.5 Pins 143 and 144

These pins are V_{SS} and V_{DD}, respectively, in the ST10F269Zx. On the ST10F276Z5 they are used as XTAL3 and XTAL4 for connection to an optional 32 kHz crystal to clock the Real Time Clock during power-down.

Hardware impact

PCB must be redesigned.

If the optional 32 kHz is not used:

- pin 143 (XTAL3) must be linked to ground like on the ST10F269Zx
- pin 144 (XTAL4) must be left open. It can also be connected to ground via a capacitor to reduce the potential RF noise that might be propagated inside the device if the pin is left floating.

Software impact

In case the optional 32 kHz is not used, the OFF32 bit of the RTCCON register must be set. Prior to setting the OFF32 bit in RTCCON register, the RTC must be enabled by setting RTCEN, bit 4 of XPERCON, and XPEN, bit 3 of SYSCON.

1.2 XRAM

The ST10F269Zx has 10 Kbytes of extension RAM whereas the ST10F276Z5 has 66 Kbytes.

The XRAM of the ST10F269Zx is divided into 2 ranges, XRAM1 of 2 Kbytes and XRAM2 of 8 Kbytes:

- The **XRAM1** address range is 00'E000h - 00'E7FFh if enabled (XPEN and XRAM1EN, bit 2 of SYSCON register and of XPERCON register, respectively, must both be set).
- The **XRAM2** address range is 00'C000h - 00'DFFFh if enabled (XPEN and XRAM2EN, bit 2 of SYSCON register and bit 3 of XPERCON register, respectively, must both be set).

The XRAM of the ST10F276Z5 is divided into 2 ranges, XRAM1 of 2 Kbytes and XRAM2 of 64 Kbytes:

- The **XRAM1** address range is 00'E000h - 00'E7FFh if enabled (XPEN and XRAM1EN, bit 2 of SYSCON register and bit 2 of XPERCON register, respectively, must both be set).
- The **XRAM2** address range is 0F'0000h - 0F'FFFFh if enabled (XPEN and XRAM2EN, bit 2 of SYSCON register and bit 3 of XPERCON register, respectively, must both be set).

1.2.1 Hardware impacts

None.

1.2.2 Software impacts

There is no change in the enabling of the XRAM blocks: XPERCON register bits, XRAM1EN and XRAM2EN, and SYSCON register bit, XPEN, are used to enable them.

The memory mapping of the application is impacted by the different XRAM size and the different location of XRAM2 in segment 15. In the ST10F269Zx the whole XRAM is in page 3 of segment 0.

Variables and PEC transfers

For architecture reasons, the PEC destination and source pointers must be in segment 0. Therefore all RAM variables and arrays that will be PEC addressed must be located within either the DPRAM (00'F600h - 00'FDFFh) or XRAM1 (00'E000h - 00'E7FFh).

About Toolchain memory model

A change in the Toolchain configuration is needed to take into account the new XRAM2 location. In the ST10F269Zx, the entire XRAM is in page 3 and is then automatically addressed using DPP3 that points to page 3 (in order to access the DPRAM and the SFR/ESFR). For the ST10F276Z5, it is necessary to dedicate a DPP to access some of XRAM2.

Example in case of Small Memory Model with Tasking toolchain

The Small memory model makes it possible to have a total code size up to 16 Mbytes, up to 64 Kbytes of fast accessible 'normal user data' in three different memory configurations and the possibility to access far/huge data, if more than 64 Kbytes of data is needed.

The three memory configurations possible for this 64 Kbytes of 'normal user data' are:

- Default

  The four DPP registers are assumed to contain their system startup value (0-3), providing one linear data area of 64 Kbytes in the first segment (00'0000h - 00'FFFFh).

- Addresses Linear

  DPP3 contains page number 3, allowing access to ST10 registers and bit-addressable memory. DPP0 - DPP2 provide a linear data area of 48 Kbytes anywhere in memory.

- Paged

  DPP3 contains page number 3, allowing access to ST10 registers and bit-addressable memory. DPP0, DPP1 and DPP2 contain the page numbers of data areas of 16 Kbytes anywhere in memory.

The Default configuration can no longer be used. The other configurations offer the following possibilities:

- with the Addresses Linear configuration the XRAM2 block is almost entirely covered with DPPs but then accesses to constants must be made via EXTP instructions.
- In the Paged configuration up to two DPPs can be assigned to XRAM2 and one DPP for constants.

1.3 Flash EEPROM

Table 2. Flash memory key characteristics

	ST10F269Zx	ST10F276Z5
Flash Size	256 Kbytes	832 KBytes
Flash Organization	7 blocks	4 banks, 17 blocks
Programming voltage	5 Volts	5 Volts
Programming method	Write/Erase Controller	Write/Erase Controller
Program/Erase cycles	100000 cycles	100000 cycles

Table 3: Flash memory mapping shows the Flash memory address ranges of the 2 devices.

Table 3. Flash memory mapping

Segment number	ST10F269Zx Flash mapping		ST10F276Z5 Flash mapping	
14	05'0000 - 0E'FFFF	External memory	0E'0000 - 0E'FFFF	Flash registers
13			0D'0000 - 0D'FFFF	X-Bank3, Block1: 64KB
12			0C'0000 - 0C'FFFF	X-Bank3, Block0: 64KB
11			0B'0000 - 0B'FFFF	X-Bank2, Block2: 64KB
10			0A'0000 - 0A'FFFF	X-Bank2, Block1: 64KB
9			09'0000 - 09'FFFF	X-Bank2, Block0: 64KB
8			08'0000 - 08'FFFF	I-Bank1, Block1: 64KB
7			07'0000 - 07'FFFF	I-Bank1, Block0: 64KB
6			06'0000 - 06'FFFF	I-Bank0, Block9: 64KB
5			05'0000 - 05'FFFF	I-Bank0, Block8: 64KB
4	04'0000 - 04'FFFF	Block6: 64KB	04'0000 - 04'FFFF	I-Bank0, Block7: 64KB
3	03'0000 - 03'FFFF	Block 5: 64KB	03'0000 - 03'FFFF	I-Bank0, Block6: 64KB
2	02'0000 - 02'FFFF	Block 4: 64KB	02'0000 - 02'FFFF	I-Bank0, Block5: 64KB
1	01'8000 - 01'FFFF	Block 3: 32KB	01'8000 - 01'FFFF	I-Bank0, Block4: 32KB
	01'0000 - 01'7FFF	External memory	01'0000 - 01'7FFF	External memory
	00'8000 - 00'FFFF	External memory Internal RAM	00'8000 - 00'FFFF	External memory Internal RAM
0	00'6000 - 00'7FFF	Block 2: 8KB	00'6000 - 00'7FFF	I-Bank0, Block3: 8KB
	00'4000 - 00'5FFF	Block 1: 8KB	00'4000 - 00'5FFF	I-Bank0, Block2: 8KB
	00'0000 - 00'3FFF	Block 0: 16KB	00'2000 - 00'3FFF	I-Bank0, Block1:8KB
			00'0000 - 00'1FFF	I-Bank0, Block0: 8KB

1.3.1 Hardware impacts

None.

1.3.2 Software impacts

The mapping of the application, the programming and erasing routines are impacted.

1.4 A/D converter

In the ST10F276Z5, the Analog Digital converter has been re-designed (compared to the A/D converter in the ST10F269Zx). The ST10F276Z5 still provides an Analog / Digital Converter with 10-bit resolution and an on-chip sample & hold circuit.

1.4.1 Hardware / Software impact: conversion timing control

The A/D Converter in the ST10F276Z5 is not fully compatible to that in the ST10F269Zx (timing and programming model).

In the ST10F269Zx, the sample time (to charge the capacitors) and the conversion time are programmable and can be adjusted to the external circuitry. The total conversion time is compatible with the formula used for ST10F269Zx, while the meanings of the ADCTC and ADSTC bit fields are no longer compatible.

Table 4. ST10F276Z5 conversion timing table

ADCTC	ADSTC	Sample	Comparison	Extra	Total Conversion
00	00	TCL * 120	TCL * 240	TCL * 28	TCL * 388
00	01	TCL * 140	TCL * 280	TCL * 16	TCL * 436
00	10	TCL * 200	TCL * 280	TCL * 52	TCL * 532
00	11	TCL * 400	TCL * 280	TCL * 44	TCL * 724
11	00	TCL * 240	TCL * 120	TCL * 52	TCL * 772
11	01	TCL * 280	TCL * 560	TCL * 28	TCL * 868
11	10	TCL * 400	TCL * 560	TCL * 100	TCL * 1060
11	11	TCL * 800	TCL * 560	TCL * 52	TCL * 1444
10	00	TCL * 480	TCL * 960	TCL * 100	TCL * 1540
10	01	TCL * 560	TCL * 1120	TCL * 52	TCL * 1732
10	10	TCL * 800	TCL * 1120	TCL * 196	TCL * 2116
10	11	TCL * 1600	TCL * 1120	TCL * 164	TCL * 2884

The parameter to take care of is the Sample time: This is the time during which the capacitances of the converter are charged via the respective analog input pins. *Table 5: ST10F276Z5 vs. ST10F269Zx sample time comparison table* shows the respective sample times of the 2 devices.

Table 5. ST10F276Z5 vs. ST10F269Zx sample time comparison table

ADCTC	ADSTC	ST10F269Zx Sample Time	ST10F276Z5 Sample Time	Ratio F276Z5 / F269Zx
00	00	TCL * 48	TCL * 120	2.5
00	01	TCL * 96	TCL * 140	1.46
00	10	TCL * 192	TCL * 200	1.04
00	11	TCL * 384	TCL * 400	1.04
11	00	TCL * 96	TCL * 240	2.5
11	01	TCL * 192	TCL * 280	1.46
11	10	TCL * 384	TCL * 400	1.04
11	11	TCL * 768	TCL * 800	1.04
10	00	TCL * 192	TCL * 480	2.08
10	01	TCL * 384	TCL * 560	1.46
10	10	TCL * 768	TCL * 800	1.04
10	11	TCL * 1538	TCL * 1600	1.04

In the default configuration the sample time of the ST10F276Z5 is 2.5 times longer compared to that of the ST10F269Zx. This has an impact on the frequency of the input signal that can be applied to the ST10F276Z5.

1.4.2 Hardware impacts

Electrical characteristics

Table 6 lists the differences in the DC characteristics of the two devices. The main points are:

- I_{AREF} is 10 times higher on the ST10F276Z5. The V_{AREF} pad must therefore be directly connected to the power supply: Connecting a resistor would create a voltage shift in the analog reference.
- C_{AIN}, input pin capacitances are different.
- DNL, INL and OFS are different: the ADC conversion curves for the 2 devices are different.

Table 6. ADC differences

Parameter	Symbol	Limit values for ST10F269Zx		Limit values for ST10F276Z5		Unit
		min.	max.	min.	max.	
Analog Reference voltage	V_{AREF}	4.0	V_{DD} + 0.1	4.5	V_{DD}	V
Analog Input Voltage	V_{AIN}	V_{AGND}	V_{AREF}	V_{AGND}	V_{AREF}	V
ADC Input capacitance Port5, Not sampling Port5, Sampling Port1, Not Sampling Port1, sampling	C_{AIN}	 - - - -	 10 15 N.A. N.A.	 - - - -	C_{P1} + C_{P2} +C_S 7 10.5 9 12.5	pF
Sample time	t_S	48TCL	1536TCL	1µs 120TCL	1600TCL	
Conversion time	t_C	388TCL	2884TCL	388TCL	2884TCL	
Total Unadjusted Error Port5 Port1 - No overload Port1 - Overload	TUE	 -2.0 - -	 +2.0 - -	 -2.0 -5.0 -7.0	 +2.0 +5.0 +7.0	LSB
Internal resistance of analog source	R_{ASRC}		t_S[ns]/150 - 0.25			kΩ
Analog switch resistance	R_{SW} Port5 Port1	N.A.	N.A.	 - -	 600 1000	Ω
	R_{AD}	N.A.	N.A.	-	1300	Ω
Reference supply current running mode power-down mode	I_{AREF}	 - -	 500 1	 - -	 5000 1	µA
Differential Nonlinearity	DNL	-0.5	+0.5	1	1	LSB
Integral Nonlinearity	INL	-1.5	+1.5	-1.5	1.5	LSB
Offset Error	OFS	-1.0	+1.0	-1.5	1.5	LSB

Note: The V_{AREF} pin is also used as a supply pin for the ADC module. As there is a higher current sink on this pin on the ST10F276Z5 compared to the ST10F269Zx, it is recommended not to connect a resistor (for example because of an RC filter), to prevent creating an offset in the reference.

1.4.3 Software impacts

Self-calibration and ADC initialization routine

An automatic self-calibration adjusts the ADC module to process parameter variations at each reset event. After reset, the busy flag (read-only) ADBSY is set because the self-calibration is ongoing. The

duration of self-calibration depends on the CPU clock: It may take up to 40.629 ± 1 clock pulses. The user must poll this bit to know when self-calibration is complete in order to initialize the ADC module.

This self-calibration is seen by the ST10F276Z5 as a conversion and thus bit ADCIR is set. The software must perform a dummy read of the ADDAT register and clear the ADCIR and ADCEIR flags before configuring the ADC module and starting the first conversion.

New bit ADOFF, bit 6 of ADCON register

ADCON (FFA0h / A0h) **SFR** **Reset Value: 0000h**

15	14	13	12	**11**	10	9	**8**	7	6	5	4	3	2	1	0
ADCTC		ADSTC		**ADCTC**	ADCIN	ADWR	**ADBSY**	ADST	ADOFF	ADM		ADCH			
RW		RW		**RW**	RW	RW	**R**	RW	RW	RW		RW			

Bit	Function	Comment
ADOFF	ADC Disable ‘0’: Analog circuitry of A/D converter is on ‘1’: Analog circuitry of A/D converter is turned off (no consumption)	New bit only for the ST10F276Z5. Reserved for the ST10F269Zx.

The bit 6 of the ADCON register, reserved in previous ST10 devices, is now used to enable or disable the ADC. By default this bit is cleared and the ST10F276Z5 is compatible with the ST10F269Zx. Therefore there is no impact on the software, provided that the software does not write to this bit.

Additional analog channels on Port1

A new multiplexer selects one out of up to 16+8 analog input channels (alternate functions of Port 5 and Port1). The selection of Port1 or Port5 as input of the ADC is made via ADCMUX, bit 0 of XMISC register. By default the multiplexer selects Port5, so there is no impact on the software as compared to an ST10F269Zx implementation.

Note that XMISCEN, bit 10 of the XPERCON register, must be set to have access to the XMISC register.

XMISC (EB46h) **XREG** **Reset Value: --00h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	VREGOFF	CANCK2	CANPAR	ADCMUX
												RW	RW	RW	RW

Bit	Function
ADCMUX	‘0’ default configuration, analog inputs on port P5.y can be converted ‘1’ analog inputs on port P1.z can be converted, only 8 channel can be managed

1.5 Real Time Clock

The RTC module can be clocked by two different sources: the main oscillator (pins XTAL1 and XTAL2) or the 32 kHz low power oscillator (pins XTAL3 and XTAL4). The selection of the clock source can be made via an additional bit in the RTCCON register.

1.5.1 Hardware impacts

Check the usage of XTAL3 and XTAL4 (respectively pins 143 and 144).

1.5.2 Software impacts

The address range of the RTC registers has been modified from 00'EC00h - 00'ECFFh on the ST10F269Zx to 00'ED00h - 00'EDFFh on the ST10F276Z5. This change had no impact if the software uses the register names defined by the toolchains and if the target CPU selection is changed to ST10F276Z5.

If the software was directly using the address of the RTC register, it must be modified according to new mapping.

In the ST10F269Zx, both byte and word accesses were allowed for the RTC module. In the ST10F276Z5, only word accesses are possible. Check that the code is not doing byte accesses to the RTC module.

In addition, new bits have been added into the RTCCON register (OSC, OFF32). There is no impact if the code was not writing to the upper part of the RTCCON register, which was reserved.

The handling of the RTCAIR and RTCSIR flags (respectively, bit 2 and bit 0 of the RTCCON register) is also changed:

- In the ST10F276Z5, these flags are cleared by writing them to 1
- In the ST10F269Zx, these flags are cleared by writing them to 0

As these flags must be cleared by software when entering the corresponding interrupt service routine, a change in the application code is needed.

Example for the RTCSIR flag

Replace ST10F269Zx code:

```
RTCCON &= 0xFFFE;// Clear RTCSIR flag
```

by the following code for ST10F276Z5:

```
RTCCON |= 0x0001;// Write 1 into RTCSIR flag to clear it
```

ST10F269Zx: RTCCON (F1C4h / E2h) ESFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	RTC OFF	-	-	-	RTC AEN	RTC AIR	RTC SEN	RTC SIR
								RW				RW	RW	RW	RW

ST10F276Z5: RTCCON (F1C4h / E2h) ESFR Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	OFF32	OSC	RTCOFF	-	-	-	RTCAEN	RTCAIR	RTCSEN	RTCSIR
						RW	R	RW				RW	RW	RW	RW

Table 7. RTCCON Register bits

Bit	Function	Reset value
RTCSIR	RTC Second Interrupt Request flag (every basic clock unit) '0': the bit was reset less than a Basic Clock unit ago. '1': the interrupt was triggered.	0
RTCSEN	RTC Second interrupt Enable '0': RTC_SecIT is disabled. '1': RTC_SecIT is enabled, it is generated every basic clock unit.	0
RTCAIR	RTC Alarm Interrupt Request flag (when the alarm is triggered) '0': the bit was reset less than n Basic Clock units ago. '1': the interrupt was triggered.	0
RTCAEN	RTC Alarm Interrupt Enable '0': RTC_alarmIT is disabled. '1': RTC_alarmIT is enabled.	0
RTCOFF	RTC Switch Off bit '0': clock oscillator and RTC run even if ST10 is in Power Down mode. '1': clock oscillator is off when ST10 enters Power Down mode. Besides, setting this bit stop RTC dividers and counters, and registers can be written.	0
OSC	Oscillator Selection Flag '0': the clock oscillator used by the RTC is the Main oscillator. '1': the clock oscillator used by the RTC is the low power 32 kHz oscillator.	U
OFF32	32 kHz Oscillator Switch Off bit '0': The 32 kHz oscillator is enabled. RTC clocked by 32 kHz oscillator (if there is a valid signal). '1': The 32 kHz oscillator is disabled. RTC clocked by the main oscillator.	0

1.6 CAN modules

The ST10F269Zx has two CAN modules of the B-CAN type.

The ST10F276Z5 has two CAN modules of the C-CAN type. These modules are functionally compatible with the modules of the ST10F269Zx.

The C-CAN cells provide additional Message Objects and new functionalities like Time Triggered Protocol capability. The main difference is that the Message Objects are no longer directly accessed as memory but are available through a Message Interface. This changes the programming model of the modules.

In the ST10F269Zx, byte and word accesses are authorized for the CAN modules. In the ST10F276Z5 only word accesses are possible.

1.6.1 Hardware impacts

None.

1.6.2 Software impacts

Re-write the CAN Drivers.

1.7 Port input control

The Port Input Control register PICON is used to select between TTL and CMOS-like input thresholds. The CMOS-like input thresholds are defined above the TTL levels and feature a hysteresis to prevent the inputs from toggling while the respective input signal level is near the thresholds.

On the ST10F269Zx this feature is available for all pins of Port 2, Port 3, Port4, Port 7 and Port 8 and the hysteresis level is 250mV for CMOS levels.

In the ST10F276Z5, Port 6 has been added. Moreover the default hysteresis is now 500mV for TTL levels and 800mV for CMOS levels.

ST10F269Zx: PICON ($F1C4_h$ / $E2_h$) ESFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	P8LIN	P7LIN	-	P4LIN	P3HIN	P3LIN	P2HIN	P2LIN
								RW	RW	-	RW	RW	RW	RW	RW

ST10F276Z5: PICON ($F1C4_h$ / $E2_h$) ESFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	P8LIN	P7LIN	P6LIN	P4LIN	P3HIN	P3LIN	P2HIN	P2LIN
								RW	RW	RW	RW	RW	RW	RW	RW

Bit	Function	Reset Value
PxLIN	Port x Low Byte Input Level Selection '0': Pins Px.7..0 switch on standard TTL input levels 1: Pins Px.7..0 switch on CMOS input levels	0
PxHIN	Port x High Byte Input Level Selection '0': Pins Px.15..8 switch on standard TTL input levels '1': Pins Px.15..8 switch on CMOS input levels	0

1.7.1 Hardware impacts

The CMOS levels of the 2 devices are slightly different, therefore the circuitry must be checked to verify that the new levels can still match the requirements. Refer to the ST10F276Z5 datasheet and to the *Section 5.1: DC characteristics* for more details.

1.7.2 Software impacts

The initialization of the PICON register should be checked to control that it is not writing to the new bit P6LIN.

1.8 Port output control

In the ST10F269Zx, the port output control registers POCONx are used to select the output driver characteristics of a port. In this way, the output drivers can be adapted to the application's requirements, and eventually, the EMI behavior of the device can be improved.

Two characteristics may be selected:

- **Edge characteristic** defines the rise/fall time for the respective outputs, that is, the transition time. Slow edge reduces the peak currents that are sunk/sourced when changing the voltage level of an external capacitive load.
- **Driver characteristic** defines either the general driving capability of the respective drivers, or if the driver strength is reduced after the target output level has been reached or not. Reducing the driver strength increases the output's internal resistance, which attenuates noise that is imported via the output line.

This feature is not available on the ST10F276Z5.

1.8.1 Hardware impacts

Depending on the usage of this functionality, some modifications might be needed.

1.8.2 Software impacts

Parts related to the initialization of the POCONx registers should be suppressed.

1.9 PLL and main on-chip oscillator

Compared to the ST10F269Zx, several modifications have been introduced:

- PLL multiplication factors have been adapted in order to match the new frequency range.
- On-chip main oscillator input frequency range has been reshaped, reducing it to a range from 4 to 12 MHz: this allows the power consumption to be reduced when the Real Time Clock is running in Power Down mode and the on-chip main oscillator clock is used as the reference.
- When the PLL is used, the CPU frequency range is 16 to 64 MHz.

Figure 1: ST10F276Z5 clock generation diagram gives a simplified description of the CPU clock generation. Depending on the multiplication factor selected via Port 0 at reset, values are set for each stage. The CPU clock is in fact generated mainly from a VCO (Voltage Controlled Oscillator) with the following characteristics:

- input range: 1 to 3.5 MHz, which is delivered from XTAL divided by a prescaler.
- output range: 64 to 128 MHz that is then divided through Divider1 to generate the CPU clock

Figure 1. ST10F276Z5 clock generation diagram

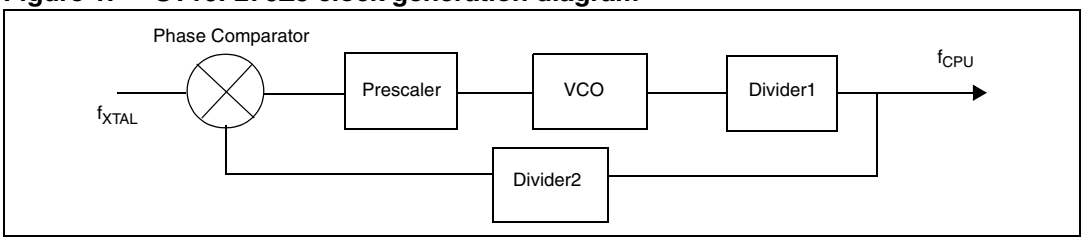

Table 8: ST10F269Zx vs. ST10F276Z5 PLL ratio lists the new PLL multiplication factors and the corresponding frequency ranges for the ST10F276Z5.

Table 8. ST10F269Zx vs. ST10F276Z5 PLL ratio

P0.15-13 (P0H.7-5)			ST10F269Zx	ST10F276Z5		Notes
			PLL factor $f_{CPU} = f_{XTAL} * F$	PLL factor $f_{CPU} = f_{XTAL} * F$	Input Frequency Range (MHz)	
1	1	1	$F_{XTAL} * 4$	$F_{XTAL} * 4$	4 to 8	Default configuration
1	1	0	$F_{XTAL} * 3$	$F_{XTAL} * 3$	5.3 to 10.6	
1	0	1	$F_{XTAL} * 8$	$F_{XTAL} * 8$	4 to 8	
1	0	0	$F_{XTAL} * 5$	$F_{XTAL} * 5$	6.4 to 12	
0	1	1	$F_{XTAL} * 1$	$F_{XTAL} * 1$	1 to 64	Direct Drive
0	1	0	$F_{XTAL} * 1.5$	$F_{XTAL} * 10$	4 to 6.4	
0	0	1	$F_{XTAL} / 2$	$F_{XTAL} / 2$	4 to 12	CPU clock via pre-scaler
0	0	0	$F_{XTAL} * 2.5$	$F_{XTAL} * 16$	4	

All configurations need a crystal (or ceramic resonator) to generate the CPU clock through the internal oscillator amplifier, except for the Direct Drive mode (oscillator amplifier disabled, so no crystal or resonator can be used). Vice versa, the clock can be forced through an external clock source only in Direct Drive mode.

1.9.1 Hardware impacts

Port 0 configuration might be changed with regards to the new PLL factor.

The components on XTAL1 & XTAL2 (crystal and capacitors, or resonator) must be changed for the following reasons:

- the input frequency range is now 4 to 12 MHz
- it is no longer possible to use a crystal or a ceramic resonator in direct drive mode
- it is no longer possible to use a PLL factor with a frequency generator
- the electrical characteristics of the main oscillator have changed (transconductance)

1.9.2 Software impact

None.

2 New features

2.1 Additional XPeripherals

Some peripherals have been added to the ST10F276Z5. They are mapped on the X-Bus and are linked to additional alternate functions of some ports of the ST10F276Z5.

The additional XPeripherals are the following:

- A second SSC (SSC of ST10F269Zx becomes SSC0, while the new one is referred to as XSSC or simply SSC1). Note that some restrictions and functional differences due to the XBUS peculiarities are present between the standard SSC, and the new XSSC.
- A second ASC (ASC0 of ST10F269Zx remains ASC0, while the new one is referred to as XASC or simply as ASC1). Note that some restrictions and functional differences due to the XBUS peculiarities are present between the standard ASC, and the new XASC.
- A second PWM (PWM of ST10F269Zx becomes PWM0, while the new one is referred to as XPWM or simply as PWM1). Note that some restrictions and functional differences due to the XBUS peculiarities are present between the standard PWM, and the new XPWM.
- An I²C interface is added (see X-I²C or simply I²C interface).

2.1.1 Hardware impacts

None if the additional XPeripherals are not used.

2.1.2 Software impacts

None if the additional Peripherals are not used. As they are XPeripherals, they can be enabled / disabled via the XPERCON and SYSCON registers. By default, the settings of XPERCON and SYSCON are compatible with the ST10F269Zx.

2.2 New multiplexer for X-Interrupts

The limited number of X-Bus interrupt lines of the present ST10 architecture, imposes some constraints on the implementation of the new functionalities. In particular, the additional XPeripherals XSSC, XASC, XI2C and XPWM need some resources to implement interrupts and PEC transfer. For this reason, a complex but very flexible multiplexed structure for the interrupt is proposed. In *Figure 2* the principle is represented through a simple diagram, which shows the basic structure replicated for each of the four X-interrupt vectors (XP0INT, XP1INT, XP2INT and XP3INT).

It is based on a new 16-bit register XIRxSEL (x=0,1,2,3), divided into two bytes:

- Higher Byte (XIRxSEL[15:8]) Interrupt Enable bits
- Lower Byte (XIRxSEL[7:0]) Interrupt Flag bits

When different sources submit an interrupt request, the enable bits (Higher Byte of XIRxSEL register) define a mask which controls which sources will be associated with the unique available vector. If more than one source is enabled to issue the request, the service routine has to identify the real event to be serviced. This can easily be done by checking the flag bits (Lower Byte of XIRxSEL register). Note that the flag bit can provide information about events which are not currently serviced by the interrupt controller (since masked through the enable bits), allowing an effective software management also in the absence of the possibility to serve the related interrupt request: a periodic polling of the flag bits may be implemented inside the user application.

Figure 2. X-Interrupt basic structure

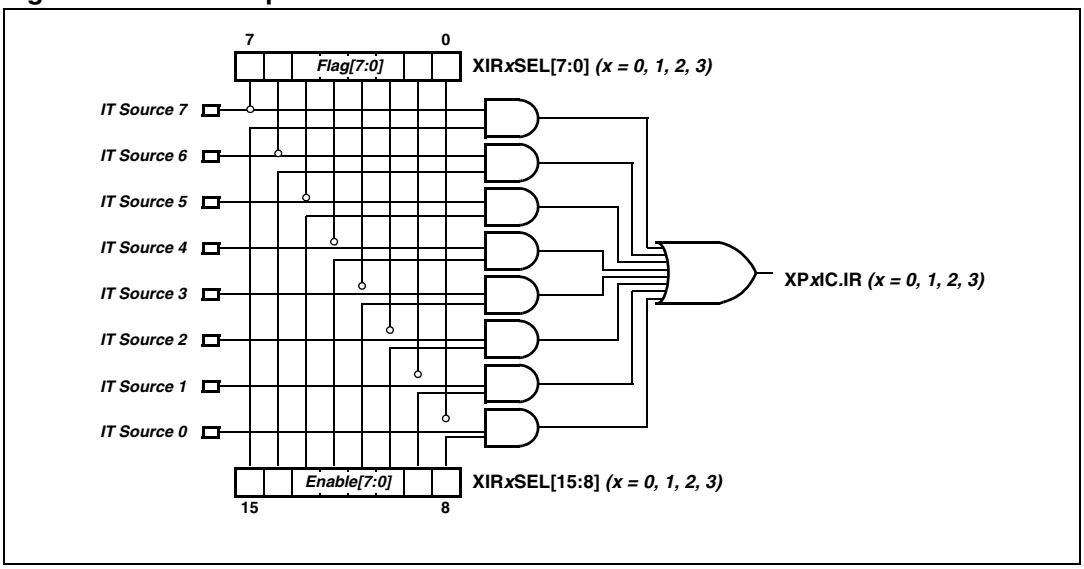

Table 9. X-Interrupt detailed mapping

	XP0INT	XP1INT	XP2INT	XP3INT
CAN1 Interrupt	X			X
CAN2 Interrupt		X		X
I2C Receive	X	X	X	
I2C Transmit	X	X	X	
I2C Error				X
SSC1 Receive	X	X	X	
SSC1 Transmit	X	X	X	
SSC1 Error				X
ASC1 Receive	X	X	X	
ASC1 Transmit	X	X	X	
ASC1 Transmit Buffer	X	X	X	
ASC1 Error				X
PLL Unlock / OWD				X
PWM1 Channel 3...0			X	X

2.2.1 Hardware impact

None.

2.2.2 Software impact

The XIRxSEL registers must be configured.

If none of the new XPeripherals is used, that is, if only the XPeripherals already present on the ST10F269Zx are used, the following values must be programmed:

- XIR0SEL = 0x0100, only the CAN1 interrupt is enabled and will generate an interrupt to the ST10 through XP0IC
- XIR1SEL = 0x0100, only the CAN2 interrupt is enabled and will generate an interrupt to the ST10 through XP1IC
- XIR2SEL = 0x0, not used
- XIR3SEL = 0x2000, only the PLL unlock interrupt is enabled and will generate an interrupt to the ST10 through XP3IC.

Then, in the interrupt routines associated with the XPxIC, the respective flags in the XIRxSEL register must be cleared. Since the XIRxSEL registers are not bit addressable, a pair of registers (a pair for each XIRxSEL) is provided to set and clear the bits of XIRxSEL without risking to overwrite requests coming after reading the register and before writing it. Therefore the following registers must be written to clear the flags:

- in the CAN1 interrupt routine, XIR0CLR (@ EB14h) = 0x0001
- in the CAN2 interrupt routine, XIR1CLR (@ EB24h) = 0x0001
- in the PLL unlock interrupt routine, XIR3CLR (@ EB44h) = 0x0020

Additional information on the X-Interrupt multiplexer structure

The *Figure 2: X-Interrupt basic structure* shows that the X-Interrupt sources are connected to the interrupt request flag of the XIRxSEL registers and to the XPxIR request flag via an AND gate with the enable bit. This AND gate is activated by a transition on the Interrupt source line and not by the latched value in the XIRxSEL register. This means that:

- A transition on the IT source line generates an interrupt to the ST10 core if the source is enabled.
- Writing to an interrupt request flag in an XIRxSEL register does not generate an interrupt to the ST10 core.

Example: If XIR0SEL = 0x0100: CAN1 interrupt enabled on XP0IC interrupt

To trigger by software the CAN1 interrupt routine with the XP0IC register, the following code must be used:

```
XIR0SET = 0x0001;/* Set CAN1 interrupt request Flag in  */
       /* XIR0SEL register */
XP0IC = XP0IC | 0x0080;/*Set XP0IR flag, generate an interrupt */
     /* routine to the ST10 */
```

Executing only the first line only sets the flag in the XIR0SEL register but it is not seen by the AND gate and cannot set the XP0IR flag.

2.3 Programmable divider on CLKOUT

A specific register mapped on the XBUS is used to choose the division factor on the CLKOUT signal (P3.15).

XCLKOUTDIV (E902h) **XBUS** **Reset Value: --00h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DIV							
								RW							

Bit	Function
DIV	$f_{CLKOUT} = f_{CPU} / (DIV + 1)$

2.3.1 Hardware impact

None.

2.3.2 Software impact

None if only CLOCKOUT is needed.

When the CLKOUT function is enabled by setting the CLKEN bit of the SYSCON register, by default the CPU clock is output on P3.15. To have access to the XCLKOUTDIV register, and thus program the clock pre-scaling factor, the XMISCEN bit of the XPERCON register and the XPEN bit of the SYSCON register must be set.

2.4 Additional port input control: XPICON register

The possibility to select between TTL and CMOS-like input thresholds has been extended to the Ports 0, 1 and 5.

ST10F276Z5: XPICON ($EB26_h$) **XREG** **Reset Value: --00h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	P5HIN	P5LIN	P1HIN	P1LIN	P0HIN	P0LIN
										RW	RW	RW	RW	RW	RW

Bit	Function	Reset Value
PxLIN	Port x Lower Byte Input Level Selection 0: Pins Px.7..0 switch on standard TTL input levels 1: Pins Px.7..0 switch on CMOS input levels	0
PxHIN	Port x Higher Byte Input Level Selection 0: Pins Px.15..8 switch on standard TTL input levels 1: Pins Px.15..8 switch on CMOS input levels	0

2.4.1 Hardware impacts

None.

2.4.2 Software impacts

None.

3 Modified registers

3.1 XPERCON register

In the ST10F276Z5, new bits have been added with regards to the additional XPeripherals.

The XPERCON register allows the XBUS peripherals to be separately selected and made visible to the user by means of the corresponding bits. If not selected (not activated with a bit of XPERCON) **before** the XPEN bit in SYSCON is set, the corresponding address space, port pins and interrupts are not occupied by the peripheral, and thus this peripheral is not visible and not available.

ST10F269Zx: XPERCON ($F024_h$ / 12_h) SFR Reset Value: --05h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	RTCEN	XRAM2EN	XRAM1EN	CAN2EN	CAN1EN
											RW	RW	RW	RW	RW

ST10F276Z5: XPERCON ($F024_h$ / 12_h) SFR Reset Value: -005h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	XMISCEN	XI2CEN	XSSCEN	XASCEN	XPWMEN	XFLASHEN	RTCEN	XRAM2EN	XRAM1EN	CAN2EN	CAN1EN
					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit number	Bit name	Function
0	**CAN1EN**	CAN1 Enable Bit '0': Accesses to the CAN1 and its functions are disabled (P4.5 and P4.6 pins can be used as general purpose IOs) '1': The CAN1 is enabled and can be accessed.
1	**CAN2EN**	CAN2 Enable Bit '0': Accesses to the CAN2 and its functions are disabled (P4.4 and P4.7 pins can be used as general purpose IOs) '1': The CAN2 is enabled and can be accessed.
2	**XRAM1EN**	XRAM1 Enable Bit '0': Accesses to the XRAM1 block are disabled, external access performed. '1': The on-chip XRAM1 is enabled and can be accessed.
3	**XRAM2EN**	XRAM2 Enable Bit '0': Accesses to the XRAM2 block are disabled, external access performed. '1': The on-chip XRAM2 is enabled and can be accessed.
4	**RTCEN**	RTC Enable Bit '0': Accesses to the Real Time Clock are disabled, external access performed. '1': The on-chip Real Time Clock is enabled and can be accessed.
5	**XFLASHEN**	XFLASH Enable Bit '0': Accesses to the on-chip XFLASH are disabled, external access performed. '1': The on-chip XFLASH is enabled and can be accessed.

Bit number	Bit name	Function
6	XPWMEN	XPWM Enable '0': Accesses to the XPWM module are disabled, external access performed. '1': The on-chip XPWM module is enabled and can be accessed.
7	XASCEN	XASC Enable Bit '0': Accesses to the XASC module are disabled, external access performed. '1': The on-chip XASC is enabled and can be accessed.
8	XSSCEN	XSSC Enable Bit '0': Accesses to the XSSC module are disabled, external access performed. '1': The on-chip XSSC is enabled and can be accessed.
9	XI2CEN	XI 2 C Enable Bit '0': Accesses to the XI2C module are disabled, external access performed. '1': The on-chip XI 2 C is enabled and can be accessed.
10	XMISCEN	XBUS Additional Features Enable Bit '0': Accesses to the Additional Miscellaneous Features are disabled. '1': The Additional Features are enabled and can be accessed.
11...15		Reserved

Accesses to the XPeripherals are configured through 3 pairs of specific XBus configuration registers, equivalent to the External Bus registers BUSCONx and ADDRSELx. Therefore several XPeripherals are sharing the same pair, with the consequence that accesses to disabled XPeripherals are only re-directed to external memory if all the XPeripherals sharing the same pair of registers are disabled.
The XPeripherals are grouped as follows:

- Group 1: CAN1, CAN2, XASC, XSSC, XI2C, XPWM, XRTC and XMISC, address range 00'E800h-00'EFFFh.
- Group 2: XRAM1, address range 00'E000h-00'E7FFh.
- Group 3: XRAM2 and XFLASH, address range 09'0000h-0F'FFFFh.

3.1.1 Hardware impacts

None.

3.1.2 Software impacts

None if the ST10F269Zx software is not writing to the reserved bit.

3.2 IDCHIP register

A new field has been added inside the IDCHIP register in order to distinguish the different peripheral options.

ST10F269Zx: IDCHIP ($F07C_h$) ESFR Reset Value: 10DXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIPID												REVID			
R												R			

ST10F276Z5: IDCHIP ($F07C_h$) ESFR Reset Value: 114Xh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCONF		CHIPID										REVID			
R		R										R			

Bit field	Function
REVID	ST10 Module Revision Identifier (Full Mask Set revision) ‘01h’: Rev. A (First main revision) ‘02h’: Rev. B (Second main revision) ... ‘0Fh’: Rev. P
CHIPID	ST10 Module Identifier ’10D’: ST10F269Zx identifier (269d = 10Dh) ‘114h’: ST10F276Z5 identifier (276d = 114h)
PCONF	Peripheral Configuration ‘00’: (E) Enhanced (ST10F276Z5) ‘01’: (B) Basic ‘10’: (D) Dedicated ‘11’: *reserved*

3.2.1 Hardware Impacts

None.

3.2.2 Software Impacts

None.

4 New registers

4.1 XADRS3 register

On previous ST10 devices, this register was already present but its value was mask programmed. On the ST10F276Z5 this register has been made available to the user. It makes it possible for the user to configure the window size and start address for the accesses to the XFlash and XRAM2 (the 2 modules are on the same XBus chip select).

ST10F276Z5: XADRS3 ($F01C_h$) SFR Reset Value: 800Bh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RGSAD												RGSZ			
RW												RW			

The register functionality is the same as that of ADDRSELx registers used for external address range selection, with some limitations:

- the address window can only be located in the first Mbyte of addressable space, that is, in the 00'0000h-0F'FFFFh range
- the window start address must be aligned to a Range Size boundary

Table 10. XADRS3 register bits

Bit number	Bit name	Function
3..0	RGSZ	Range Size Selection Defines the size of the address window.
15..4	RGSAD	Range Start Address Defines the bits A19..A8 of the start address of the address window.

Table 11. Definition of address area

Bit field RGSZ	Selected window size	Relevant bit (R) of RGSAD	Selected range Start Address Relevant bit (R) of Address (A23 - A0)
0 0 0 0	256 bytes	RRRR RRRR RRRR	0000 RRRR RRRR RRRR xxxx xxxx
0 0 0 1	512 bytes	RRRR RRRR RRRx	0000 RRRR RRRR RRRx xxxx xxxx
...	...	...	...
1 0 1 0	256 Kbytes	RRxx xxxx xxxx	0000 RRxx xxxx xxxx xxxx xxxx
1 0 1 1	512 Kbytes	Rxxx xxxx xxxx	0000 Rxxx xxxx xxxx xxxx xxxx
1 1 x x	Reserved		

4.1.1 Hardware impacts

None.

4.1.2 Software impacts

None if the XADRS3 register is not reprogrammed: the default value gives access to the entire XFlash and XRAM2 modules.

XADRS3 cannot be changed after executing the EINIT instruction.

4.2 XPEREMU register

This register has been added as a write-only register.

ST10F276Z5: XPEREMU ($EB7E_h$) XREG Reset Value: XXXXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	XMISCEN	XI2CEN	XSSCEN	XASCEN	XPWMEN	XFLASHEN	XRTCEN	XRAM2EN	XRAM1EN	CAN2EN	CAN1EN
-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W

The bit meaning is exactly the same as for the XPERCON register.

4.2.1 Hardware Impacts

None.

4.2.2 Software Impacts

Once the XPEN bit of the SYSCON register is set and at least one of the XPeripherals (except for memories) is activated, the XPEREMU register must be written with the same content as that of XPERCON: this is mandatory to allow the correct emulation of the new set of features introduced on the X-BUS for the new ST10 generation. The following instructions must be added inside the initialization routine:

```
if (SYSCON.XPEN && (XPERCON & 0x07D3))
then { XPEREMU = XPERCON }
```

Of course, XPEREMU must be programmed after XPERCON and after SYSCON, in this way the final configuration for XPeripherals is stored in XPEREMU and used for the emulation hardware setup.

4.3 Emulation-dedicated registers

A set of four additional registers is implemented for emulation purposes only. Like XPEREMU, they are write-only registers.

XEMU0 (00’EB76h)

XEMU1 (00’EB78h)

XEMU2 (00’EB7Ah)

XEMU3 (00’EB7Ch)

These registers are used by emulators. They have no user action on the ST10F276Z5.

4.3.1 Hardware impact

None.

4.3.2 Software impact

None. On the ST10F269Zx, the 00'E800h to 00'EBFFh address range was mapped onto external memory but it was recommended to reserve this space for upward compatibility.

4.4 XMISC register

ST10F276Z5: XMISC ($EB46_h$) XREG Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	VREGOFF	CANCK2	CANPAR	ADCMUX
-	-	-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW

Bit number	Bit name	Function
0	**ADCMUX**	Port1L ADC Channels Enable '0': Analog inputs on port P5.y can be converted (default configuration) '1': Analog inputs on port P1.z can be converted. Only 8 channels can be managed
1	**CANPAR**	CAN Parallel Mode Selection '0': CAN2 is mapped on P4.4/P4.7, while CAN1 is mapped on P4.5/P4.6 '1': CAN1 and CAN2 are mapped in parallel on P4.5/P4.6. This is effective only if both CAN1 and CAN2 are enabled by setting the CAN1EN and CAN2EN bits in the XPERCON register. If CAN1 is disabled, CAN2 remains on P4.4/P4.7 even if the CANPAR bit is set.
2	**CANCK2**	CAN Clock divider by 2 disable '0': Clock provided to CAN modules is CPU clock divided by 2 (mandatory when f_{CPU} is higher than 40 MHz) '1': Clock provided to CAN modules is directly CPU clock
3	**VREGOFF**	Main Voltage Regulator disable in Power-Down mode '0': Default value after reset and when Power Down is not used '1': Main Regulator is turned off when Power-Down mode is entered
4...15		Reserved

4.4.1 Hardware impact

None.

4.4.2 Software impact

None.

On the ST10F269Zx, the CAN clock is the CPU clock but it is divided by 2 when calculating the time quantum.

5 Electrical characteristics

5.1 DC characteristics

5.1.1 Absolute maximum ratings

They are the same.

5.1.2 Overview of the DC characteristics

The pads of the ST10F276Z5 have been redesigned according to the new technology and therefore the characteristics are different. User should verify the DC characteristics.

Table 12 lists the parameters that might be impacted most.

Table 12. DC characteristics

Parameter	Symbol	ST10F269Zx Limit Values		ST10F276Z5 Limit Values		Unit
		min.	max.	min.	max.	
Input low voltage	V_{IL}**SR** V_{ILS}**SR**	-0.5 -0.5	0.2 V_{DD} - 0.1 2.0, special thresholds	-0.3 -0.3	0.8 0.3 V_{DD}	V
Input low voltage ($\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, and $\overline{RPD}$)	V_{IL1}**SR**	N.A.	N.A.	-0.3	0.3 V_{DD}	V
Input low voltage (XTAL1 and XTAL3)	V_{IL2}**SR**			-0.3	0.3 V_{DD}	V
Input high voltage	V_{IH}**SR** V_{IHS}**SR**	0.2 V_{DD} + 0.9 0.8 V_{DD} - 0.2	V_{DD} + 0.5 V_{DD} + 0.5, special threshold	2.0 0.7 V_{DD}	V_{DD} + 0.3 V_{DD} + 0.3	V
Input high voltage ($\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, and $\overline{RPD}$)	V_{IH1}**SR**	0.2 V_{DD} + 0.9 0.8 V_{DD} - 0.2	V_{DD} + 0.5 V_{DD} + 0.5, special threshold	2 0.7 V_{DD}	V_{DD} + 0.3 V_{DD} + 0.3	V
Input high voltage XTAL1	V_{IH2}**SR**	0.7 V_{DD}	V_{DD} + 0.5	0.7 V_{DD}	V_{DD} + 0.3	V
Input Hysteresis	HYS	N.A. 250, special threshold	-	400 750	700 1400	mV
Input Hysteresis $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$	V_{HYS1}**CC**			750	1400	mV
Output low voltage	V_{OL}**CC**	PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$	0.45 / I_{OL} = 2.4mA	PORT6, ALE, CLKOUT, $\overline{WR}$, READY, $\overline{BHE}$, $\overline{RD}$, $\overline{RSTOUT}$, $\overline{RSTIN}$	0.4 / I_{OL} = 8mA 0.05 / I_{OL} = 1mA	V

Table 12. DC characteristics

Parameter	Symbol	ST10F269Zx Limit Values		ST10F276Z5 Limit Values		Unit
		min.	max.	min.	max.	
Output low voltage (all other)	V_{OL1}**CC**	–	0.45 / I_{OL} = 1.6mA	–	0.4 / I_{OL} = 4 mA 0.05 / I_{OL} = 0,5 mA	V
Output high voltage	V_{OH}**CC**	0.9V_{DD} / I_{OH} = -0.5 mA 2.4 / I_{OH} = -2.4 mA	PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$	V_{DD} - 0.8 / I_{OH} = -8 mA V_{DD} -0.08 / I_{OH} = -1 mA	PORT6, ALE, CLKOUT, $\overline{WR}$, READY, $\overline{BHE}$, $\overline{RD}$, $\overline{RSTOUT}$, $\overline{RSTIN}$	V
Output high voltage (all other)	V_{OH1}**CC**	0.9V_{DD} / I_{OH} = -0.25 mA 2.4 / I_{OH} = -1.6 mA	–	V_{DD} - 0.8 / I_{OH} = -4 mA V_{DD} -0.08 / I_{OH} = -0.5 mA	–	V
Input leakage current (Port5)	I_{OZ1}**CC**	–	± 200	–	± 200	nA
Input leakage current (all other)	I_{OZ2}**CC**	–	±1	–	±0.5	uA
Input leakage current (P2.0)	I_{OZ3}**CC**	–	-	–	-0.5 +1	uA
Input leakage current (RPD)	I_{OZ4}**CC**	–	-	–	±3	uA
Overload current (P2.0)	I_{OV2}**CC**	–	-	–	-1 +5	mA

5.2 AC characteristics at 40 MHz

As the technology is different between the two devices, the I/Os also present some differences in the AC behavior. *Table 13* and *Table 14* list all the timing differences. Please check carefully your design for possible impact.

5.2.1 External memory bus timings

Note that for high CPU clock frequencies above 40 MHz (when using the ST10F276Z5Q3), some numbers in the timing formulas become zero or negative, that in most of the cases is not acceptable or not meaningful at all. In these cases, it is necessary to reduce the speed of the bus setting properly t_A (ALE extension), t_C (Memory Cycle Time wait-states) and t_F (Memory tri-state time).

Multiplexed bus

Table 13. Multiplexed bus timings (ns)

Symbol	Parameter	ST10F269Zx		ST10F276Z5		ST10F269Zx f_{CPU} = 40MHz		ST10F276Z5 f_{CPU} = 40MHz	
		min.	max.	min.	max.	min.	max.	min.	max.
t_6 **CC**	Address setup to ALE	TCL - 10.5 + t_A	-	TCL - 11 + t_A	-	2 + t_A	-	1.5 + t_A	-
t_{16} **SR**	ALE low to valid data in	-	3 TCL - 19 + t_A + t_C	-	3 TCL - 20 + t_A + t_C	18.5 + t_A + t_C	-	17.5 + t_A + t_C	-
t_{17} **SR**	Address/Unlatched $\overline{CS}$ to valid data in	-	4 TCL - 28 + 2t_A + t_C	-	4 TCL - 30 + 2t_A + t_C	22 + 2t_A + t_C	-	20 + 2t_A + t_C	-
t_{39} **SR**	Latched $\overline{CS}$ low to Valid Data In	-	3 TCL - 19 + 2t_A + t_C	-	3 TCL - 21 + 2t_A + t_C	18.5 + 2t_A + t_C	-	16.5 + 2t_A + t_C	-
t_{44} **CC**	Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	-	0	-	1.5	-	0	-	1.5
t_{45} **CC**	Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	-	TCL	-	TCL + 1.5	-	12.5	-	14

Demultiplexed bus

Table 14. Multiplexed bus timings

Symbol	Parameter	ST10F269Zx		ST10F276Z5		ST10F269Zx f_{CPU} = 40 MHz		ST10F276Z5 f_{CPU} = 40 MHz	
		min.	max.	min.	max.	min.	max.	min.	max.
t_6CC	Address setup to ALE	TCL - 10.5 + t_A	-	TCL - 11 + t_A	-	2 + t_A	-	1.5 + t_A	-
t_{80}CC	Address/Unlatched $\overline{CS}$ setup to $\overline{RD}$, $\overline{WR}$ (with RW delay)	-	2 TCL - 8.5 + 2t_A	-	2 TCL - 12.5 + 2t_A	16.5 + 2t_A	-	12.5 + 2t_A	-
t_{81}CC	Address/Unlatched $\overline{CS}$ setup to $\overline{RD}$, $\overline{WR}$ (no RW delay)	-	TCL - 8.5 + 2t_A	-	TCL - 12 + 2t_A	4 + 2t_A	-	0.5 + 2t_A	-
t_{16}SR	ALE low to valid data in	-	3 TCL - 19 + t_A + t_C	-	3 TCL - 20 + t_A + t_C	18.5 + t_A + t_C	-	17.5 + t_A + t_C	-
t_{17}SR	Address/Unlatched $\overline{CS}$ to valid data in	-	4 TCL - 28 + 2t_A + t_C	-	4 TCL - 30 + 2t_A + t_C	22 + 2t_A + t_C	-	20 + 2t_A + t_C	-

Table 14. Multiplexed bus timings (continued)

Symbol	Parameter	ST10F269Zx		ST10F276Z5		ST10F269Zx f_{CPU} = 40 MHz		ST10F276Z5 f_{CPU} = 40 MHz	
		min.	max.	min.	max.	min.	max.	min.	max.
t_{28}CC	Address/Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	0 (no t_F) -5 + t_F (t_F > 0)	-	0 + t_F	-	0 (no t_F) -5 + t_F (t_F > 0)	-	0 + t_F	-
t_{39}SR	Latched $\overline{CS}$ low to valid data in	-	3 TCL - 19 + $2t_A$ + t_C	-	3 TCL - 21 + $2t_A$ + t_C	18.5 + $2t_A$ + t_C	-	16.5 + $2t_A$ + t_C	-
t_{82}CC	Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	2 TCL - 10.5 + $2t_A$	-	2 TCL - 11 + $2t_A$	-	14.5 + $2t_A$	-	14 + $2t_A$	-

5.2.2 Hi-Speed Synchronous Serial Interface (SSC)

The Maximum Baudrate of the SSC in the ST10F276Z5 is 8 Mbaud whereas it is of 10 in the ST10F269Zx. For CPU frequencies strictly higher than 32 MHz, the minimum value of the SSCBR register (prescaler value) must not be lower than 2.

6 Revision history

Table 15. Revision history

Date	Revision	Changes
06-July-2007	1	Initial release

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